WE CLAIM:

1. A source synchronous CDMA bus interface, comprising:

a single data channel;

at least one data transmitter circuit coupled to said data channel at a first point;

at least one data receiver circuit coupled to said data channel at a second point;

a system clock line which runs adjacent and parallel to said data channel; and

a system clock signal applied to said system clock line such that said system clock signal propagates in parallel with data sent from said at least one data transmitter circuit to said at least one data receiver circuit via said data channel;

each of said data transmitter circuits comprising:

a first clock signal generating circuit coupled at its input to said system clock line at a point approximately adjacent to said first point, said first clock generating circuit arranged to generate a first clock signal derived from said system clock signal;

a modulating circuit connected to receive base-band data to be transmitted via said data channel at a first input and a unique orthogonal code at a second input and to produce data modulated by said unique orthogonal code at an output; and

a transmitter connected to receive said modulated data and said first clock at respective inputs and which is arranged to use said first clock to align said modulated data with said system clock signal and to provide said aligned modulated data at an output which is coupled to said data channel at said first point such that said aligned modulated data is transmitted using source

synchronous clocking;

each of said data receiver circuits comprising:

a second clock signal generating circuit coupled at its input to said system clock line at a point approximately adjacent to said second point, said second clock generating circuit arranged to generate a second clock signal derived from said system clock signal;

a receiver coupled to said data channel at said second point such that it receives said aligned modulated data and said second clock at respective inputs and which is arranged to use said second clock to align said received data with said system clock signal; and

a demodulating circuit connected to receive said aligned received data at a first input and said unique orthogonal code at a second input and to produce data demodulated with said orthogonal code at an output and thereby recover said base-band data.

2. The bus interface of claim 1, wherein said first and second clock generating circuits are delay-locked-loop (DLL) circuits.

3. The bus interface of claim 1, wherein said first and second clock generating circuits are phase-locked-loop (PLL) circuits.

4. The bus interface of claim 1, wherein said orthogonal codes are Walsh codes.

5. The bus interface of claim 1, wherein said at least one data transmitter circuit and said at least one data receiver circuit comprise at least two data transmitter circuits and at least two data receiver circuits, each of said modulating circuits receiving

respective unique orthogonal codes and each of said demodulating circuits corresponding to one of said modulating circuits and receiving said modulating circuit's orthogonal code, said unique orthogonal codes enabling the aligned modulated data from said at least two data transmitter circuits to be conveyed via said single data channel to said at least two data receiving circuits simultaneously.

6. The bus interface of claim 5, wherein said at least two data transmitter circuits share said first clock signal and the outputs of said at least two data transmitter circuits are connected together at a common node which is coupled to said data channel at said first point.

7. The bus interface of claim 5, wherein the outputs of said at least two data transmitter circuits are coupled to said data channel at different points along said data channel, each of said data transmitter circuits having respective first clock circuits, the input of each first clock circuit connected to said system clock line at a point approximately adjacent to where said first clock circuit's data transmitter circuit is coupled to said data channel, such that the outputs of said data transmitter circuits are transmitted using source synchronous clocking and superposed in said data channel.

8. The bus interface of claim 5, wherein said at least two data receiver circuits share said second clock signal and the inputs of said at least two data receiver circuits are connected together at a common node which is coupled to said data channel at said second point.

9. The bus interface of claim 5, wherein the inputs

of said at least two data receiver circuits are coupled to said data channel at different points along said data channel, each of said data receiver circuits having respective second clock circuits, the input of each second clock circuit connected to said system clock line at a point approximately adjacent to where said second clock circuit's data receiver circuit is coupled to said data channel.

10. The bus interface of claim 5, further comprising a system controller which provides said unique orthogonal codes to said data transmitter circuits and said data receiving circuits such that aligned modulated data coupled to said data channel is received and demodulated by a specific data receiver circuit, said system controller thereby configuring said bus interface.

11. The bus interface of claim 5, wherein said at least two data transmitter circuits and said at least two data receiver circuits comprise two data transmitter circuits and two data receiver circuits which are arranged such that said aligned modulated data employs 3-PAM signaling when data from said two data transmitter circuits is simultaneously conveyed via said single data channel to said two data receiver circuits.

12. The bus interface of claim 11, wherein said orthogonal codes are 2-bit Walsh codes.

13. The bus interface of claim 5, wherein said at least two data transmitter circuits and said at least two data receiver circuits comprise four data transmitter circuits and four data receiver circuits which are arranged such that said aligned modulated data employs 5-PAM signaling when data from said four data transmitter

circuits is simultaneously conveyed via said single data channel to said four data receiver circuits.

14. The bus interface of claim 13, wherein said orthogonal codes are 4-bit Walsh codes.

15. The bus interface of claim 1, wherein said system clock line runs adjacent and parallel to said data channel in a first direction, reverses direction and continues adjacent and parallel to said data channel in a second direction opposite said first direction, said system clock signal applied to said system clock line such that said system clock signal propagates down said system clock line in said first direction and continues down said system clock line is said second direction.

16. The bus interface of claim 15, wherein said data channel conveys data bi-directionally between said data transmitter circuits and said data receiver circuits, a data transmitter circuit conveying data to a data receiver circuit in said first direction having their respective clock generating circuit inputs connected to respective points on the portion of said system clock line running in said first direction, and a data transmitter circuit conveying data to a data receiver circuit in said second direction having their respective clock generating circuit inputs connected to respective points on the portion of said system clock line running in said second direction.

17. The bus interface of claim 1, wherein said data channel is parallel terminated at each end.

18. The bus interface of claim 1, wherein said data channel is a transmission line.

19. The bus interface of claim 1, further comprising at least one data storage device interfaced to at least one of said data transmitter circuits such that said bus interface provides a memory bus which conveys data from said at least one data storage device to said at least one data receiver circuit.

20. The bus interface of claim 19, further comprising at least one CPU interfaced to at least one of said data receiver circuits such that said memory bus conveys data from said at least one data storage device to said at least one CPU.

21. The bus interface of claim 19, further comprising at least one memory controller interfaced to at least one of said data receiver circuits such that said memory bus conveys data from said at least one data storage device to said at least one memory controller.

22. The bus interface of claim 1, wherein said modulating circuit comprises at least one exclusive-OR gate connected to receive said base-band data and said unique orthogonal code at respective inputs and to produce said modulated data at said output, said modulated data cd0(t) given by:

$cd0(t) = D0(t) \oplus C0(t)$,

wherein D0(t) is said base-band data and C0(t) is said unique orthogonal code.

23. The bus interface of claim 1, wherein said transmitter comprises an output driver having a current-mode open-drain structure.

24. The bus interface of claim 1, wherein said at

least one data transmitter circuit and at least one data receiver circuit comprise two data transmitter circuits and two data receiver circuits, each of said modulating circuits receiving respective unique orthogonal codes and each of said demodulating circuits corresponding to one of said modulating circuits and receiving said modulating circuit's orthogonal code, said unique orthogonal codes enabling the aligned modulated data from said two data transmitter circuits to be conveyed via said single data channel to said two data receiving circuits simultaneously using 3-PAM signaling, said receiver comprising first and second 2-bit interleaving analog-to-digital converters (ADCs) for handling even and odd data, respectively, each of said 2-bit ADCs receiving two DC reference voltages such that said ADC converts said 3-PAM signal to thermometer coded data.

25. The bus interface of claim 24, wherein said demodulating circuit comprises a plurality of exclusive-OR gates connected to receive said even and odd thermometer coded data and said unique orthogonal codes and to de-spread said thermometer coded data using said unique orthogonal codes.

26. The bus interface of claim 25, wherein said demodulating circuit further comprises a plurality of integrator circuits connected to receive said de-spread even and odd thermometer coded data and to integrate said data.

27. The bus interface of claim 26, wherein said demodulating circuit further comprises a plurality of sense amplifier flip-flops (SAFF) connected to receive, amplify, and latch said integrated data and to recover said base-band data.

28. A source synchronous CDMA bus interface suitable for use as a memory bus which provides 2-to-2 multiple access communications, comprising:

a single data channel;

first and second data transmitter circuits coupled to said data channel;

first and second data receiver circuits coupled to said data channel;

a system clock line which runs adjacent and parallel to said data channel; and

a system clock signal applied to said system clock line such that said system clock signal propagates in parallel with data sent from said data transmitter circuits to said data receiver circuits via said data channel;

each of said data transmitter circuits comprising:

a first clock signal generating circuit coupled at its input to said system clock line at a point approximately adjacent to where said data transmitter circuit is coupled to said data channel, said first clock generating circuit arranged to generate a first clock signal derived from said system clock signal;

a modulating circuit connected to receive base-band data to be transmitted at a first input and a unique orthogonal code at a second input and to produce data modulated by said unique orthogonal code at an output; and

a transmitter connected to receive said modulated data and said first clock at respective inputs and which is arranged to use said first clock to align said modulated data with said system clock signal and to provide said aligned modulated data at an output which is coupled to said data channel such that said aligned modulated data is transmitted using source synchronous clocking;

said data transmitter circuits coupling their respective aligned modulated data into said data channel simultaneously such that said data is transmitted using 3-PAM signaling;

each of said data receiver circuits comprising:

a second clock signal generating circuit coupled at its input to said system clock line at a point approximately adjacent to where said data receiver circuit is coupled to said data channel, said second clock generating circuit arranged to generate a second clock signal derived from said system clock signal;

a receiver coupled to said data channel such that it receives said aligned modulated data and said second clock at respective inputs and which is arranged to use said second clock to align said received data with said system clock signal; and

a demodulating circuit connected to receive said aligned received data at a first input and the orthogonal code provided to a given one of said modulating circuits at a second input and to produce data demodulated with said orthogonal code at an output, thereby recovering the base-band data modulated by said given modulating circuit.

29. The bus interface of claim 28, wherein said first and second clock generating circuits are delay-locked-loop (DLL) circuits.

30. The bus interface of claim 28, wherein said orthogonal codes are 2-bit Walsh codes.